

WHAT IS CLAIMED IS:

1 1. A single instruction, multiple data (SIMD) controller for processing a
2 plurality of data streams in a digital subscriber line (DSL) system, comprising:
3 a plurality of circular buffer circuits coupled to store data from said plurality
4 of data streams;
5 a plurality of address generation circuits coupled to access said data stored in
6 said plurality of circular buffer circuits;
7 a plurality of processor circuits coupled to process said data accessed by said
8 plurality of address generation circuits; and
9 a program control unit coupled to control said plurality of processor circuits
10 with an instruction.

1 2. The controller of claim 1, wherein one of said plurality of circular
2 buffer circuits comprises:
3 a first section coupled to store one or more symbols before being processed;
4 a second section coupled to store said one or more symbols being processed;
5 and
6 a third section coupled to store said one or more symbols after being
7 processed.

1 3. The controller of claim 1, wherein one of said plurality of address
2 generation circuits comprises:
3 a symbol manager circuit coupled to generate an input base address, a
4 processor base address, and an output base address,
5 wherein said one of said plurality of address generation circuits is further
6 coupled to receive an input offset address, a processor offset address, and an output offset
7 address, and to generate an input address, a processor address, and an output address in
8 accordance with said input base address, said processor base address, and said output base
9 address.

1 4. The controller of claim 1, wherein said plurality of processor circuits
2 are further coupled to receive a plurality of enable signals and to selectively process said data
3 based on said plurality of enable signals.

1 5. The controller of claim 1, wherein said plurality of address generation
2 circuits are further coupled to selectively generate a plurality of enable signals, depending
3 upon whether a full symbol is ready for processing in each of said plurality of address
4 generation circuits.

1 6. The controller of claim 5, wherein said plurality of processor circuits
2 are further coupled to receive said plurality of enable signals and to selectively process said
3 data based on said plurality of enable signals.

1 7. The controller of claim 1, wherein said plurality of address generation
2 circuits are further coupled to selectively generate a plurality of enable signals, depending
3 upon a difference between an input base address and a processor base address in each of said
4 plurality of address generation circuits.

1 8. A method of processing a plurality of data streams in a digital
2 subscriber line (DSL) system, comprising the acts of:

3 calculating a plurality of input addresses for said plurality of data streams
4 based on a plurality of input base addresses and a plurality of input offset addresses;

5 storing a plurality of data from said plurality of data streams according to said
6 plurality of input addresses;

7 calculating a plurality of processor addresses for the stored plurality of data
8 based on a plurality of processor base addresses and a plurality of processor offset addresses;

9 processing, using a single instruction, the stored plurality of data according to
10 said plurality of processor addresses;

11 calculating a plurality of output addresses for the processed plurality of data
12 based on a plurality of output base addresses and a plurality of output offset addresses;

13 outputting the processed plurality of data according to said plurality of output
14 addresses; and

15 updating said plurality of input base addresses, said plurality of processor base
16 addresses, and said plurality of output base addresses.

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